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Claims

[c1] 1. A method for fabricating a non-volatile memory, comprising:
providing a substrate with a stacked structure having a control gate, a barrier layer, a trapping layer, and a tunneling layer, wherein an anti-reflection layer covers the stacked structure on top;
forming an oxide layer on an exposed surface of the of the control gate;
forming an insulating spacer on a sidewall of the stacked structure, and covering the oxide layer; and
forming an ultraviolet-resistant lining layer over the surface of the stacked structure.

[c2] 2. The method of claim 1, wherein the insulating spacer is a silicon oxide spacer.

[c3] 3.The method of claim 1, wherein the ultraviolet-resistant lining layer is a silicon nitride lining layer.

[c4] 4. The method of claim 3, wherein the step of forming the silicon nitride lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 370W and 410W,

the PECVD using a reacting gas including a SiH_4 gas with a flow rate between 50 sccm and 60 sccm, an NH_3 gas and a N_2 gas.

[c5] 5.The method of claim 1, wherein the anti-reflection layer includes inorganic material, so that the anti-reflection layer is not removed during removing the photoresist layer and the oxide layer is formed on sidewalls of the control gate.

[c6] 6. The method of claim 1, wherein the anti-reflection layer includes organic material, so that the anti-reflection layer is simultaneously removed during removing the photoresist layer and the oxide layer is formed on top and sidewalls of the control gate.

[c7] 7. The method of claim 1, wherein the oxide layer is formed by performing a thermal oxidation process.

[c8] 8. The method of claim 1, further forming a source/drain region in the substrate at each side of the stacked structure.

[c9] 9.A fabrication process for metal interconnects, comprising:

providing a substrate, the substrate having a conducting structure;

forming a dielectric layer on the substrate to cover the

conducting structure;
forming a contact window in the dielectric layer, the contact window being electrically connected to the conducting structure;
forming a conducting line structure on the dielectric layer, the conducting line structure being electrically connected to the contact window; and
forming a low surface charge lining layer on surfaces of the dielectric layer and the conducting line structure.

[c10] 10.The method of claim 9, wherein the low surface charge lining layer is one of a silicon oxide lining layer and a silicon nitride lining layer.

[c11] 11.The method of claim 10, wherein the step of forming the silicon oxide lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 80W and 120W, the PECVD using a reacting gas including a silane (SiH_4) gas with a flow rate between 20sccm and 30sccm, and a nitrous (N_2O) gas.

[c12] 12.The method of claim 9, further comprising forming a second dielectric layer on the low surface charge lining layer.

[c13] 13.A method for fabricating a non-volatile memory,

comprising:

sequentially forming a tunneling layer, a trapping layer, a barrier layer, a gate conductive layer, and an anti-reflection layer on a substrate;

forming a photoresist layer with a pattern on the anti-reflection layer;

using the photoresist layer as a mask to etch the anti-reflection layer, the gate conductive layer, the barrier layer, the trapping layer, and the tunneling layer, to form a stacked structure having a control gate, the barrier layer, the trapping layer, and the tunneling layer, wherein the anti-reflection layer covers the stacked structure on top;

removing the photoresist layer;

forming an oxide layer on an exposed surface of the of the control gate;

forming a source/drain region in the substrate at each side of the stacked structure;

forming an ultraviolet-resistant lining layer over the stacked structure;

forming a dielectric layer on the ultraviolet-resistant lining layer;

forming a contact window in the dielectric layer, the contact window being electrically connected to the control gate;

forming a conducting line structure on the dielectric

layer, the conducting line structure being electrically connected to the contact window; and
forming a low-surface-charge lining layer over the dielectric layer and the conducting line structure

[c14] 14. The method of claim 13, wherein the insulating spacer is a silicon oxide spacer.

[c15] 15.The method of claim 13, wherein the ultraviolet-resistant lining layer is a silicon nitride lining layer.

[c16] 16. The method of claim 15, wherein the step of forming the silicon nitride lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 370W and 410W, the PECVD using a reacting gas including a silane (SiH_4) gas with a flow rate between 50sccm and 60sccm, an ammonium (NH_3) gas and a nitroge (N_2) gas.

[c17] 17.The method of claim 13, wherein the low-surface-charge lining layer is one of a silicon oxide lining layer and a silicon nitride lining layer.

[c18] 18.The method of claim 17, wherein the step of forming the silicon oxide lining layer further comprises performing a plasma enhanced chemical vapor deposition (PECVD) process with a power between 80W and 120W, the PECVD using a reacting gas including a SiH_4gas with

a flow rate between 20sccm and 30sccm, and an NO_2 gas.

[c19] 19.The method of claim 13, wherein the anti-reflection layer includes inorganic material, so that the anti-reflection layer is not removed during removing the photoresist layer and the oxide layer is formed on sidewalls of the control gate.

[c20] 20. The method of claim 13, wherein the anti-reflection layer includes organic material, so that the anti-reflection layer is simultaneously removed during removing the photoresist layer and the oxide layer is formed on top and sidewalls of the control gate.

[c21] 21. The method of claim 13, wherein the oxide layer is formed by performing a thermal oxidation process.

[c22] 22.The method of claim 13, further comprising forming a second dielectric layer on the low-surface-charge lining layer.